

MSX RS232C interface hardware specification

ASCII Microsoft
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This document describes the hardware requirements of RS-232C interface for MSX home personal computers.

1.0 LSI COMPONENTS

- i-8251 Communication interface
- i-8253 Programmable interval timer

At least 4Kbyte of ROM storage for the support software.

2.0 PORT ADDRESS

80H	R/W	8251 data port
81H	R/W	8251 command/status port
82H	R	Status sense port for CTS, Timer/Counter 2, RI and CD
82H	W	Interrupt mask register
83H		* Not specified
84H	R/W	8253 counter 0
85H	R/W	8253 counter 1
86H	R/W	8253 counter 2
87H	W	8253 mode register

* The port whose address is 83H can be used for the manufacturer's own purpose.

3.0 THE USAGE OF PORT AT ADDRESS 82H

82H read - Get system status

data bit	Description
D7	CTS (Clear To Send) 0 - CTS is asserted 1 - CTS is negated
D6	Timer/counter output-2 from i8253
D5	---+
D4	
D3	Reserved
D2	---+
D1	+ RI (Ring Indicator) 0 - RI is asserted 1 - RI is negated
D0	+ CD (Carrier Detect) 0 - CD is asserted 1 - CD is negated

NOTE: Signals with + sign are optional. If only one of them is implemented, it must be a 'CD' signal.

NOTE

The CTS is not sensed through 8251, but sensed through the port as described above because of the problem in CTS logic in some version of 8251 and make the software handling possible.

82H write - Interrupt mask register

data bit	Description
D7	---+
D6	
D5	Reserved
D4	---+
D3	+ Timer interrupt from i8253 channel-2 1 - mask interrupt (initial value) 0 - enable interrupt
D2	+ Sync character detect/Break detect 1 - mask interrupt (initial value) 0 - enable interrupt
D1	+ Transmit data ready (TxReady) 1 - mask interrupt (initial value) 0 - enable interrupt
D0	Receive data ready (RxReady) 1 - mask interrupt (initial value) 0 - enable interrupt

NOTE: Signals with + sign are optional. That is, the minimum requirement for the interrupt signal is RxReady.

4.0 THE USAGE OF 8253 TIMER-COUNTER TO GENERATE BAUD RATE CLOCK FOR 8251

4.1 Frequency Of X'tal

The frequency of the crystal:
1.8432MHz

baud rate (baud)	scale factor and error (x16)
50	2304
75	1536
110	1047 110.0287 +0.3%
150	768
300	384
600	192
1200	96
1800	64
2000	58 1986.2 -0.7%
2400	48
3600	32
4800	24
7200	16
9600	12
19200	6

4.2 The Usage Of Counter Channel

CH0 - Rx baud rate clock
 CH1 - Tx baud rate clock
 CH2 - Used by application
 Optionally generates interrupt

5.0 THE CONNECTION OF DB25 CONNECTOR

PIN	SIGNAL	PIN	SIGNAL
1	Frame ground	14	
2	Transmit data	15	
3	Receive data	16	
4	Request To Send	17	
5	Clear To Send	18	
6	Data Set Ready	19	
7	Signal ground	20	Data Terminal Ready
8	Carrier detect	21	
9		22	Ring Indicator
10		23	
11		24	
12		25	
13			

MSX Multiple Channel RS232C Interface Hardware Specification

4th October, 1985
2nd November, 1985

(All information contained herein is proprietary to ASCII MSFE)

This document describes the hardware requirements of multi channel RS-232C interface for MSX computers.

1.0 LSI COMPONENTS

i-8251 Communication interface

i-8253 Programmable interval timer to generate receiver/transmitter clock.

2KByte of RAM storage for the receiver queue buffer and work area.

Minimum 8Kbyte of ROM storage for the support software.

2.0 ROM, RAM, I/O ADDRESS

2.1 The Address Of ROM Which Contains Control Program

The RS-232C control program is located between 4000H and 5FFFH. This program handles extended BASIC statements and devices, and extended BIOS calls. The maximum number of channels which can be supported is 4 channels per one cartridge, and 4 channels per one system.

2.2 The Address Of RAM For Work Area

The RAM is placed between 6000H and 67FFH. The same RAM can also be accessed from location A000H to A7FFH. Thus if you write 1 to address 6000H, A000H also becomes 1. Therefore the RAM address decoder must be designed so that the control program is able to access the RAM from both locations. This configuration maximizes the execution speed of the control program.

The RAM area is used to:

- a) keep receiver queue buffer whose size is 256 byte (128 characters including error information) per one channel.
- b) store flags and variables
- c) keep communication parameters

2.3 I/O Port Address

To support the multiple channel of RS-232C, all the hardware is placed in the memory address space to prevent the address collision. However, to support the old application program which accesses the I/O port directly, a channel can also be accessed through I/O port, and this feature can be controlled by the software.

Memory address	I/O address		
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BFF8H	80H	R/W	8251 data port
BFF9H	81H	R/W	8251 command/status port
BFFAH	82H	R	Status for CTS, Timer/Counter 2, RI and CD
BFFAH	82H	W	Interrupt mask register
BFFBH	83H		* Not specified
BFFCH	84H	R/W	8253 counter 0
BFFDH	85H	R/W	8253 counter 1
BFFEH	86H	R/W	8253 counter 2
BFFFH	87H	W	8253 mode register

Above memory address is for the channel 0. The top address of channel 1 is BFF0H, channel 2 is BFE8H and channel 3 is BFE0H. The channels must be contiguous and must start from 0.

Good combinations

- o Channel 0 only
- o Channel 0 and 1
- o Channel 0, 1 and 2
- o Channel 0, 1, 2 and 3

Bad combinations

- o Channel 0 and 2
- o Channel 0 and 3
- o Channel 1 only
- o Channel 1 and 2
- o Channel 1, 2 and 3
- o Channel 3 only
- o Etc.

The channel 0 is a special channel, which has an 'I/O port enable bit (bit 4 of BFFAH)'. When the bit is 1, the channel 0 can be accessed via I/O port specified above. This is to keep the compatibility with the old I/O port only type of RS-232C interface.

The control program first looks for the existence of RS-232C interface in the I/O address space. If it failed to find one, it sets the bit 4 of BFFAH to 1 to enable the access through I/O port to the channel 0. Thus old application program which accesses the RS-232C hardware directly through the I/O port is still able to access the I/O port from 80H to 87H directly.

The contents of the I/O port 82H is the same as BFFAH except for the bit 4. This bit can not be accessed from I/O port 82H to prevent accidentally turning off the bit by the application software that disables the access through I/O address space.

The port whose address is BFFBH(memory)/83H(I/O) can be used by the manufacturer for their own purpose such as MODEM control.

2.4 Address Map

Memory map

4000H+	Control program ROM (8K byte minimum)
6000H+	Work area RAM (2K byte)
6800H+	Not used
8000H+	Not used
A000H+	The image of the Work area RAM
A800H+	Not used
BFE0H+	Channel-3 I/O area if exists
BFE8H+	Channel-2 I/O area if exists
BFF0H+	Channel-1 I/O area if exists
BFF8H+	Channel-0 I/O area
BFFFH	

I/O map

80H+	Channel-0 I/O area
87H	if enabled

3.0 THE USAGE OF PORT AT ADDRESS BFFAH(MEMORY)/82H(I/O)

Read - Get system status

data bit	Description
D7	CTS (Clear To Send) 0 - CTS is asserted 1 - CTS is negated
D6	Timer/counter output-2 from i8253
D5	---
D4	---
D3	Reserved
D2	---
D1	+ RI (Ring Indicator) 0 - RI is asserted 1 - RI is negated
D0	+ CD (Carrier Detect) 0 - CD is asserted 1 - CD is negated

NOTE: Signals with + sign are optional. If only one of them is implemented, it must be a 'CD' signal.

NOTE

The CTS is not sensed through 8251, but sensed through the port as described above because of the problem in CTS logic in some version of 8251 and make the software handling possible.

Write - Interrupt mask register

data bit	Description
D7	---
D6	Reserved (These bits are set to 1)
D5	---
D4	Enable access to the ch0 thru I/O port (BFFAH only) 1 - enable access through I/O port 0 - disable access through I/O port
D3	+ Timer interrupt from i8253 channel-2 1 - mask interrupt (initial value) 0 - enable interrupt
D2	+ Sync character detect/Break detect 1 - mask interrupt (initial value) 0 - enable interrupt
D1	+ Transmit data ready (TxReady) 1 - mask interrupt (initial value) 0 - enable interrupt
D0	Receive data ready (RxReady) 1 - mask interrupt (initial value) 0 - enable interrupt

NOTE: Signals with + sign are optional. That is, the minimum requirement for the interrupt signal is RxReady.

4.0 THE USAGE OF I8253 TIMER-COUNTER

4.1 Frequency Of X'tal

The frequency of the crystal:
1.8432MHz

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4.2 The Usage Of Counter Channel

CH0 - Rx baud rate clock
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5.0 THE CONNECTION OF DB25 CONNECTOR

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11		24	
12		25	
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